

REMARKS

Claims 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by applicant admitted prior art (AAPA)(Fig.2).

5 Claims 7-9 are rejected under 35 U.S.C. 102(a) as being anticipated by Rostoker et al. (6,407,434). Claims 1-6 are rejected under 35 U.S.C 103(a) as being obvious over AAPA(Fig.2, [0006]-[0007]) in view of Rostoker et al. (6,407,434) or Sercu et al., "STUDY OF GRIDGING AND CELL-CELL INTERACTIONS IN THE
10 METHOD OF MOMENTS ANALYSIS OF ARBITRARILY SHAPED PLANAR CIRCUITS", IEEE, 1993, PP. 753-756.

1. Response to the rejection of claims 7-9 under 35 U.S.C. 102(b):

15

Please first refer to Fig.3 of this application. This application discloses a method of dividing a semiconductor integrated circuit pattern. The method discloses depicting a dividing line 34 to divide the polygonal planar 36 into the
20 unit figures 38, the unit figures 38 only arranged sequentially and horizontally. Besides, the dividing line 34 also divides the unit figures 38 of the polygonal planar 36 into at least two regions, having two adjacent unit figures being respectively divided into different regions.

25

Next, please refer to Fig.2 of this application. The AAPA discloses first depicting a horizontal line 16 to divide the polygonal planar 14 into a top portion 14a and a bottom portion 14b. Then, a plurality of vertical line segments 18 must be
30 formed so as to divide the polygonal planar 14 into a plurality of unit figures 20. So, the AAPA just teaches how to divide the polygonal planar 14 into a plurality of unit figures 20.

Thereof some of the unit figures 20 is arranged sequentially and horizontally, some of the unit figures 20 is arranged sequentially and vertically..

5 In conclusion, the AAPA discloses dividing the polygonal planar 14 into unit figures 20, some of the unit figures 20 arranged sequentially and horizontally and some of the unit figures 20 arranged sequentially and vertically. This application discloses dividing the polygonal planar 14 into
10 unit figures 20 that are only arranged sequentially and horizontally. Therefore, features in the claims 7-9 are novel and never disclosed, so consideration of the claims 7-9 is politely requested.

15 2. Response to the rejection of claims 7-9 under 35 U.S.C. 102(a):

Rostoker et al. discloses a cell architecture used for the IC layout. The cell architectures include triangles,
20 rectangles, trapezoids, parallelograms, and other shapes (col.6, lines 6-11, & col.85 lines 1-67).

However, this application discloses a method to divide the semiconductor circuit pattern into a plurality of unit figures
25 so as to convert a semiconductor circuit pattern data into input graphic data of a writer, and then the writer is able to use the input graphic data to draw the circuit pattern on a photo mask or a substrate.

30 Therefore, the disclosure of Rostoker et al. and the disclosure of this application are applied to the different fields. Therefore, features in the claims 7-9 are novel and

never disclosed, so consideration of the claims 7-9 is politely requested.

3. Response to the rejection of claims 1-6 under 35 U.S.C.
5 103(a):

Sercu et al. discloses first dividing the polygonal planar circuit into triangular and rectangular cells. The cell-cell interaction is then calculated (pp.753, Abstract).

10

However, this application discloses a method to divide the semiconductor circuit pattern into a plurality of unit figures so as to convert a semiconductor circuit pattern data into input graphic data for a writer, and then the writer is able
15 to use the input graphic data to draw the circuit pattern on a photo mask or a substrate.

20

So the disclosure of Sercu et al. and the disclosure of this application are applied to the different fields.

25

Further, as mentioned above, the AAPA and this application disclose different dividing methods, and the disclosure of Rostoker et al. and the disclosure of this application are applied to the different fields.

30

In conclusion, the rejection over AAPA in view of Rostoker et al. or Sercu et al. is not suitable for this application. So consideration of claims 1-6 is politely requested.

Sincerely,

5 Winston Hsu Date: 1/19/2004

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506

Merrifield, VA 22116

U.S.A.

10 e-mail : winstonhsu@naipo.com.tw

(Please contact me by e-mail if you need a telephone communication and I will return your call promptly.)